

1 **What is claimed is:**

2 1. A method for communicating data between a processor and one or
3 more devices over an IDE bus, comprising the steps of:

4 connecting three or more devices to an IDE bus;

5 configuring each device as Cable Select; and

6 providing a device controller that selectively activates at most two of the
7 devices at the same time for data communication over the IDE bus.

8
9 2. The method of claim 1, further comprising the steps of, the device
10 controller:

11 identifying one or two devices for data communication with the processor;

12 selecting a first of the identified devices as a master device;

13 if more than one device identified, then selecting the second of the
14 identified devices as a slave device; and

15 activating each selected device, such that a maximum of only two devices
16 are active at the same time, whereby the activated devices can communicate
17 with the processor over the IDE bus.

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19 3. The method of claim 2, further comprising the steps of, the device
20 controller receiving identity of said devices for data communication from the
21 processor.

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23 4. The method of claim 1, wherein the device controller is configured
24 to activate a maximum of two of said three or more devices connected to the IDE
25 bus at a time, and to deactivate the remaining of said three or more devices.

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27 5. The method of claim 4, wherein the device controller is configured
28 to activate said maximum of two devices by powering the two devices on, and to
29 deactivate said remaining devices by powering said remaining devices off.

1 6. The method of claim 1, wherein the device controller is configured
2 to select each of said two devices via a selection signal for each of said two
3 devices.

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5 7. The method of claim 6, wherein said selection signal comprises the
6 IDE Cable Select line of each device.

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8 8. The method of claim 1, wherein at least one of the devices on the
9 IDE bus comprises a disk drive.

10
11 9. A method for communicating data between a processor and three
12 or more devices over an IDE bus, comprising the steps of:

- 13 (a) deactivating all the devices;
14 (b) identifying one or two of the devices for data communication with
15 the processor;
16 (c) selecting a first of the identified devices as a master device;
17 (d) if more than one device identified, selecting the second of the
18 identified devices as a slave device;
19 (e) activating each selected device, such that a maximum of only two
20 devices are active at the same time; and
21 (f) communicating data between the processor and each activated
22 device, over the IDE bus.

23
24 10. The method of claim 9, further comprising the step of:

- 25 (g) deactivating all of the devices.

26
27 11. The method of claim 9, further comprising the steps of repeating
28 steps (a) through (f).

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30 12. The method of claim 9, further comprising the steps of, before step
31 (a), connecting three or more IDE devices to the IDE bus.

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2 13. The method of claim 9, further comprising the steps of, before step
3 (a), configuring each device as Cable Select.

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5 14. The method of claim 13, wherein:
6 step (c) further comprises the steps of selecting the first identified device
7 as a master device via the Cable Select signal for that first device; and
8 step (d) further comprises the steps of selecting the second identified
9 device as a slave device via the Cable Select signal for that second device.

10
11 15. The method of claim 9, wherein:
12 in step (a) deactivating each device includes the steps of powering each
13 device off; and
14 in step (e) activating each selected device includes the steps of powering
15 each selected device on.

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17 16. The method of claim 9, wherein at least one of the devices on the
18 IDE bus comprises a disk drive.

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20 17. An Integrated Device Electronics (IDE) interface system for
21 managing data communication between a processor and three or more devices
22 connected to an IDE bus, the IDE interface system comprising:
23 a device controller for receiving device control signals to select at least
24 one of said devices for data communication with the processor;
25 wherein the device controller selectively activates at most two of the
26 devices at the same time for data communication with the processor over the IDE
27 bus.

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29 18. The IDE interface system of claim 17, wherein the device controller
30 is configured to: (a) receive a signal from the processor to select one or two of
31 the devices identified for data communication, (b) in response to the signal,

1 select one of the identified devices as a master device; (c) if more than one
2 device identified, then select the second of the identified devices as a slave
3 device; and (d) activate each selected device, such that a maximum of only two
4 devices are active at the same time, whereby the activated devices can
5 communicate with the processor over the IDE bus.
6

7 19. The IDE interface system of claim 17, wherein the device controller
8 is configured to activate a maximum of two of said three or more devices
9 connected to the IDE bus at a time, and to deactivate the remaining of said three
10 or more devices.
11

12 20. The IDE interface system of claim 19, wherein the device controller
13 is configured to activate said maximum of two devices by powering the two
14 devices on, and to deactivate said remaining devices by powering said remaining
15 devices off.
16

17 21. The IDE interface system of claim 17, wherein the device controller
18 is configured to select each of said two devices via a selection signal for each of
19 said two devices.
20

21 22. The IDE interface system of claim 21, wherein said selection signal
22 comprises the IDE cable select line of each device.
23

24 23. The IDE interface system of claim 17, further comprising an
25 interface controller connected to said devices via the IDE bus, wherein the
26 interface controller manages information flow between the processor and said
27 devices over the IDE bus.
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29 24. The IDE interface system of claim 17, wherein at least one of the
30 devices on the IDE bus comprises a disk drive.
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1 25. A data storage system comprising:
2 three or more storage devices connected to an IDE bus for data
3 communication with a processor over the IDE bus; and
4 a device controller connected to the devices, the device controller for
5 receiving device control signals to select at least one of said devices for data
6 communication with the processor, wherein the device controller selectively
7 activates at most two of the devices at the same time for data communication
8 with the processor over the IDE bus.
9

10 26. The data storage system of claim 25, wherein the device controller
11 is configured to: (a) receive a signal the processor to select one or two of the
12 devices identified for data communication, (b) in response to the signal, select
13 one of the identified devices as a master device; (c) if more than one device
14 identified, then select the second of the identified devices as a slave device; and
15 (d) activate each selected device, such that a maximum of only two devices are
16 active at the same time, whereby the activated devices can communicate with
17 the processor over the IDE bus.
18

19 27. The data storage system of claim 25, wherein the device controller
20 is configured to activate a maximum of two of said three or more devices
21 connected to the IDE bus at a time, and to deactivate the remaining of said three
22 or more devices.
23

24 28. The data storage system of claim 27, wherein the device controller
25 is configured to activate said maximum of two devices by powering the two
26 devices on, and to deactivate said remaining devices by powering said remaining
27 devices off.
28

29 29. The data storage system of claim 25, wherein the device controller
30 is configured to select each of said two devices via a selection signal for each of
31 said two devices.

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2 30. The data storage system of claim 29, wherein said selection signal
3 comprises the IDE cable select line of each device.
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5 31. The data storage system of claim 25, further comprising an
6 interface controller connected to said devices via the IDE bus, wherein the
7 interface controller manages information flow between the processor and said
8 devices over the IDE bus.
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10 32. The data storage system of claim 25, wherein at least one of the
11 devices on the IDE bus comprises a disk drive.